Abstract

Carbon nanotube Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) provides better scalability and performance with suppressed short-channel effects and higher carrier mobility as compared to the conventional silicon MOSFET. Carbon is therefore a strong candidate to replace silicon as the fundamental building material of integrated circuits in the future. Several novel techniques for achieving high-performance and low-power integrated circuits with carbon nanotube transistors are proposed in this dissertation.

Domino logic circuits are commonly employed for enhanced speed on the critical signal propagation paths of integrated circuits. A novel variable strength keeper technique is proposed for achieving robust, high-speed, and low-leakage domino logic circuits with carbon nanotube transistors. High-performance NP dynamic CMOS circuits are also explored. The well-known area and power consumption disadvantages of the NP dynamic CMOS circuits are eliminated by employing a carbon nanotube transistor technology. A 32-bit NP dynamic CMOS adder with carbon nanotube transistors occupies smaller area and consumes significantly lower power while providing similar speed as compared to the traditional silicon domino adders.

The amount of on-die memory cache is increased to enhance the performance of modern systems-on-chip. Static Random-Access Memory (SRAM) cell is the basic building block of on-chip memory. A novel SRAM cell with nine carbon nanotube transistors is proposed for achieving enhanced reliability and energy-efficiency in future memory circuits. With the new SRAM cell, the read and write voltage margins are enhanced by up to 99.09% and 4.57x, respectively, as compared to the conventional memory circuits in a 16nm carbon nanotube transistor technology. Furthermore, the leakage power consumption of an idle 1Kibit SRAM array is reduced by up to 34.18% with the new SRAM cell as compared to the conventional memory cells. Formation of metallic carbon nanotubes due to diameter variations produces short-circuits in the channel arrays of transistors, thereby causing malfunction. A new memory design technique that is tolerant to the unwanted formations of metallic carbon nanotubes is also presented in this dissertation for achieving higher memory-yield with robust read and write operations.