TEMPERATURE ADAPTIVE AND
VARIATION TOLERANT CMOS CIRCUITS

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The imbalanced utilization and the diversity of circuitry cause on-chip temperature gradients. Different sections of high-performance integrated circuits typically operate at different temperatures. Furthermore, environmental temperature fluctuations can cause significant variations in the die temperature. Temperature fluctuations alter the speed characteristics of CMOS circuits. Several techniques to reduce the sensitivity of circuit speed to the fluctuations of die temperature are proposed in this dissertation. The techniques simultaneously target temperature variation resilience and enhanced energy efficiency in CMOS circuits. A generic power measurement methodology to accurately evaluate the energy savings provided with the proposed techniques is also presented.

The drain current produced by a MOSFET operating at the prescribed nominal supply voltage is reduced at elevated temperatures primarily due to the degradation of carrier mobility. New voltage optimization techniques are described in this dissertation to provide temperature variation insensitive constant transistor current with the standard CMOS technologies. The optimum supply and threshold voltages that achieve temperature variation insensitive constant circuit speed are identified for different technologies. The energy savings provided with the two proposed temperature variation tolerant voltage optimization techniques are compared.

Low power design methodologies are typically aimed to reduce the energy consumption or the energy-delay product in CMOS integrated circuits. The propagation
delays of circuits optimized for minimum energy consumption and minimum energy-delay product are highly sensitive to temperature fluctuations. Alternatively, the voltage optimization techniques explored in this dissertation simultaneously achieve enhanced energy efficiency and temperature variation tolerance. The speed and energy tradeoffs in circuits operating at the supply voltages that provide temperature variation insensitive performance, minimum energy consumption, and minimum energy-delay product are presented.

Integrated circuits with ultra-low-voltage power supplies exhibit reversed temperature dependence. The speed of circuits optimized for minimum energy consumption is enhanced at elevated temperatures. New temperature-adaptive dynamic supply and threshold voltage tuning techniques are proposed in this dissertation to enhance the high temperature energy efficiency of ultra-low-voltage CMOS circuits. The objective is achieved by either dynamically scaling the power supply voltage or dynamically increasing the device threshold voltages through reverse body-bias. The energy savings provided with the two temperature-adaptive voltage tuning techniques are presented.