Temperature-Adaptive Body-Bias and Supply Voltage Scaling for Enhanced Energy Efficiency in Nano-CMOS Circuits

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Abstract – Temperature dependent propagation delay characteristics of CMOS circuits will experience a complete reversal in the near future. Contrary to the older technology generations, the speed of standard zero-body-biased circuits in a 32nm CMOS technology is enhanced when the temperature is increased at the nominal supply voltage. The enhancement of circuit speed provides new opportunities to lower the energy consumed by active circuits at elevated temperatures. Temperature-adaptive supply and threshold voltage tuning techniques are proposed in this paper to reduce the high temperature active mode energy consumption without degrading the circuit speed. Results indicate that the energy consumption can be lowered by up to 21% by dynamically scaling the supply voltage at elevated temperatures. An alternative technique based on temperature-adaptive reverse body-bias exponentially reduces the leakage currents as well as the parasitic junction capacitances of the MOSFETs. The temperature-adaptive threshold voltage tuning through reverse body-bias yields an active mode energy reduction by up to 29.8% as compared to the standard zero-body-biased circuits at high temperatures.

1. INTRODUCTION

Process and environment parameter variations in scaled CMOS technologies are posing greater challenges in the design of reliable integrated circuits. Because of the imbalanced utilization and diversity of circuitry, temperature can vary significantly from one die area to another [1]. Furthermore, environmental temperature fluctuations can cause significant variations in the die temperature. For example, electronic systems mounted on automobile engines operate at a temperature range from -40°C to 150°C [2]. Variations in the die temperature affect the device and wire characteristics, thereby altering the performance of integrated circuits.

The supply voltage in a new technology generation is determined based on the target clock frequency, power consumption budget, and device reliability requirements [3]-[4]. Scaling the device dimensions strengthens the electric fields between device terminals while lowering the parasitic capacitances, thereby enhancing the speed of CMOS integrated circuits. The speed of a circuit can be further enhanced by scaling the threshold voltages. Due to the subthreshold leakage current constraints, however, the threshold voltages are scaled at a much slower rate as compared to the supply voltage. The supply voltage to threshold voltage ratio is reduced with each new technology generation. The variation of the threshold voltage therefore plays an increasingly important role in determining the MOSFET drain current variations when the temperature fluctuates. As discussed in [3], a complete reversal in the temperature dependent speed characteristics of CMOS circuits will be observed in the near future.

Dynamic supply voltage scaling technique is primarily used for reducing the active mode power consumption of an integrated circuit by exploiting the variations in the computational workload [4]-[6]. Alternatively, adaptive body-bias technique reduces both the active and standby mode power consumption by dynamically adjusting the device threshold voltages depending on the variations of the workload and the circuit activity [4], [6]. In this paper, new temperature-adaptive dynamic supply and threshold voltage tuning techniques are proposed to reduce the energy consumption of active CMOS circuits at elevated temperatures. In a circuit that exhibits reversed temperature dependence, the high temperature energy efficiency can be enhanced without degrading the circuit speed, either by dynamically scaling the supply voltage or by reverse body-biasing the devices in the circuit. The optimum power supply and body-bias voltages that lower the energy consumption without degrading the circuit speed at increased temperatures are identified in this paper for circuits in a 32nm CMOS technology. The active mode energy savings provided with the two temperature-adaptive dynamic voltage tuning techniques are compared.

The paper is organized as follows. The effects of temperature fluctuations on the device and circuit characteristics at the nominal supply voltage under standard zero-body-bias conditions are examined in Section 2. The new temperature-adaptive supply and threshold voltage scaling techniques for reducing the energy consumed at high die temperatures are described in Section 3. The energy reduction offered with the temperature-adaptive design methodologies are compared in Section 4. Finally, some conclusions are provided in Section 5.

2. DEVICE AND CIRCUIT BEHAVIOR UNDER TEMPERATURE FLUCTUATIONS

The effects of temperature fluctuations on the device and circuit characteristics are reviewed in this section. An increase in the die temperature degrades the absolute values of threshold voltage, carrier mobility, and saturation velocity of MOSFETs [3], [7]-[8]. The saturation velocity is typically a weak function of temperature [8]. Threshold voltage degradation with temperature tends to enhance the drain current because of the increase in gate overdrive \( V_{GS} - V_t \). Alternatively, degradation in carrier mobility tends to lower the MOSFET drain current [7]. Effective variation of MOSFET drain current is determined by the variation of the dominant device parameter when the temperature fluctuates [3]. Temperature fluctuation induced gate overdrive and carrier mobility variations at the nominal supply voltage for zero-body-biased devices in a 32nm CMOS technology [9] are listed in Table 1.

In older technology generations with higher supply to threshold voltage ratio, the variation of primarily the carrier
mobility determines the MOSFET current when the temperature fluctuates at the nominal supply voltage [3]. The MOSFET drain current and the circuit speed are, therefore, reduced following the degradation of carrier mobility when the temperature is increased at the nominal voltage [3].

### Table I

<table>
<thead>
<tr>
<th>Technology</th>
<th>Gate Overdrive (V)</th>
<th>Carrier Mobility (x10⁻² m²/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>32nm CMOS Technology</td>
<td>PMOS</td>
<td>NMOS</td>
</tr>
<tr>
<td>25°C</td>
<td>-0.286</td>
<td>0.275</td>
</tr>
<tr>
<td>125°C</td>
<td>-0.399</td>
<td>0.398</td>
</tr>
<tr>
<td>Variation (%)</td>
<td>39.63</td>
<td>44.85</td>
</tr>
</tbody>
</table>

The amount of heat dissipated by an integrated circuit is dependent on the switching activity and the power consumption [4]. Die temperature is further determined by the variations in the ambient temperature where a circuit is deployed. Higher die temperature exponentially increases the leakage currents [4]. Increased leakage power, inturn, further enhances the heat dissipation and elevates the die temperature. This positive feedback between the die temperature, leakage current, and the total power consumption accelerates the degradation of the device/circuit reliability due to excessive heating and can cause thermal runaway. New temperature-adaptive design methodologies are, therefore, highly desirable to enhance the reliability and energy efficiency of deeply scaled nanometer CMOS circuits.

In this paper, temperature-adaptive supply and threshold voltage tuning techniques are proposed to dynamically adjust the circuit speed based on the die temperature. The primary objective of the proposed temperature-adaptive schemes is to lower the high temperature energy consumption without degrading the circuit speed by either dynamically scaling the power supply voltage or dynamically increasing the device threshold voltages through reverse body-bias.

### A. TEMPERATURE-ADAPTIVE DYNAMIC SUPPLY VOLTAGE SCALING

The temperature-adaptive dynamic supply voltage tuning technique is presented in this section. Both dynamic switching and leakage energy consumption are more than quadratically reduced by scaling the supply voltage of a circuit. The propagation delay of a circuit is also strongly dependent on the supply voltage [4]. Scaling the supply voltage reduces the energy consumed by a circuit at the cost of degraded circuit performance.

In nanometer CMOS circuits that exhibit reversed temperature dependence, the supply voltage of a circuit can be dynamically scaled at elevated temperatures without degrading the circuit speed. The supply voltage can be tuned until the high temperature circuit performance at the scaled supply voltage matches the circuit performance at the nominal voltage and the lowest operating temperature. Unlike the conventional work-load adaptive dynamic voltage scaling techniques [4]-[6], a new die-temperature-adaptive dynamic voltage scaling technique is proposed in this paper for tuning the circuit supply voltage based on the fluctuations of the die temperature and the circuit speed.

The normalized high temperature propagation delay of circuits at different scaled supply voltages along with the propagation delay at room temperature (25°C) and nominal supply voltage (V_{DD} = 0.7V) are shown in Fig. 2. The appropriate
amount of voltage scaling for maintaining the circuit speed is marked with a demarcation line in Fig. 2. The scaled optimum supply voltages ($V_{DD,\text{opt}}$) that maintain the circuit speed at high temperatures are 10% (carry select adder and Brent-Kung adder) to 11.4% (array multiplier) lower than the nominal supply voltage in this technology, as shown in Fig. 2.

The normalized high temperature energy consumption at the scaled optimum and the standard nominal supply voltages are shown in Fig. 3. As shown in Fig. 3, the high temperature energy consumption is reduced by 19.1% (carry select adder and Brent-Kung adder) to 21% (array multiplier) with the temperature-adaptive dynamic supply voltage scaling technique as compared to the standard single-static-supply-voltage circuit operation at the nominal voltage.

![Normalized Delay](image)

**Fig. 2.** Normalized propagation delay of circuits at different supply voltages and temperatures.

![Normalized Energy](image)

**Fig. 3.** Normalized high temperature (125°C) energy consumption at the nominal and the scaled optimum supply voltages.

**B. TEMPERATURE-ADAPTIVE BODY BIAS**

The temperature-adaptive threshold voltage tuning technique is presented in this section. Similar to the dependence on the supply voltage, the propagation delay of a circuit is also strongly dependent on the device threshold voltages [4]. The absolute value of the threshold voltages degrade as the temperature increases, thereby simultaneously enhancing the circuit speed and the subthreshold leakage currents at elevated temperatures [4], [7]. In scaled nanometer CMOS circuits that exhibit reversed temperature dependence, the threshold voltages of the devices can be adjusted at elevated temperatures to reduce the leakage current while satisfying the circuit speed benchmark. The device threshold voltages can be dynamically increased until the high temperature circuit performance matches the circuit performance with the nominal supply and zero body-bias threshold voltages at the lowest operating temperature.

The threshold voltage can be dynamically increased by reverse body-bias [4]. Applying reverse body-bias reduces the subthreshold leakage current while increasing the junction leakage due to enhanced band-to-band tunneling. For small-to-moderate body-bias voltages, the reduction in the subthreshold leakage is typically substantially higher as compared to the increase in the band-to-band tunneling current, as described in [4]. The source and drain-to-body junction capacitances of reverse body-biased devices are also reduced, thereby further enhancing the active mode energy efficiency as compared to a standard zero body-biased circuit. Unlike the conventional body-bias techniques aimed at altering the device threshold voltages based on the variations of the workload and circuit activity [4], [6], a new temperature-adaptive body-bias technique is proposed in this paper for altering the threshold voltages of the devices based on the fluctuations of the die temperature and the circuit speed.

The temperature-adaptive body-bias technique is applied to the three test circuits operating at the nominal supply voltage ($V_{DD} = 0.7V$). All the devices in the circuits are dynamically reverse body-biased to suppress the active mode leakage current at elevated temperatures. The normalized high temperature propagation delay at different body-bias voltages along with the propagation delay of the standard zero body-biased circuits at room temperature (25°C) is shown in Fig. 4. The optimum reverse body-bias (RBB) voltages required to maintain the circuit speed at elevated temperatures are from 0.12V (Brent-Kung adder) to 0.14V (carry select adder and array multiplier), as shown in Fig. 4.

The high temperature active mode energy consumption of the reverse body-biased circuits are compared to the standard zero body-biased circuits in Fig. 5. The energy consumed at the optimum body-bias voltages are normalized to the energy consumed by the corresponding zero body-biased circuit at 125°C. As shown in Fig. 5, the high temperature active mode energy consumption is reduced by 23.3% (Brent-Kung adder) to 29.8% (array multiplier) with the temperature-adaptive body-bias technique as compared to the standard zero body-biased circuits.

![Normalized Delay](image)

**Fig. 4.** Normalized propagation delay for different body-bias voltages and temperature. RBB is the absolute value of the reverse body-bias voltage ($V_{SB}$) applied to all the devices in the circuits. ZBB: Standard zero-body-bias.

**4. HIGH TEMPERATURE ENERGY REDUCTION WITH THE TEMPERATURE-ADAPTIVE SCHEMES**

The tradeoffs in the implementation of the temperature-adaptive voltage tuning schemes are presented in this section. A comparison of the percent energy reduction provided with the two temperature-adaptive schemes is shown in Fig. 6. The
high temperature energy savings offered with the temperature-adaptive reverse body-bias technique is up to 1.4x higher as compared to the temperature-adaptive dynamic supply voltage tuning technique, as shown in Fig. 6. Static energy consumption due to leakage currents is projected to exceed the dynamic switching energy in the near future [4], [10]. Increasing the device threshold voltages through reverse body-bias reduces the leakage currents as well as the device junction parasitic capacitances. The temperature-adaptive reverse body-bias technique is therefore very effective to lower the energy consumed by the active CMOS circuits at high temperatures, as shown in Fig. 6. The effectiveness of the technique would be further enhanced if the die temperature spectrum is wider than 25°C→125°C due to the deployment of a circuit in an extreme environment with more significant fluctuations in the ambient temperature.

Fig. 6. Comparison of the percent energy reduction provided with the two proposed temperature-adaptive schemes.

The proposed temperature-adaptive schemes can be implemented in a standard n-well or p-well CMOS technology. The temperature-adaptive energy reduction schemes require an energy efficient high resolution voltage scaling power supply because of the low nominal and optimum supply and body-bias voltages associated with the deeply-scaled nanometer CMOS circuits. The energy overheads related with modifying the voltage of the high parasitic capacitance of the substrate (or the wells) and the power distribution network and with generating the different body-bias and power supply voltages should be further investigated to evaluate the net system-level energy reduction provided with the proposed temperature-adaptive techniques.

The variation of the temperature of a die is typically a slow process as discussed in [11]. Because of the gradual fluctuations of the die temperature over time and a wide range of ambient temperatures experienced depending on the circuit activity and where the circuit is deployed, a finer-temperature-grain supply or threshold voltage tuning technology can be employed. The adaptation of the circuit speed to the intermediate die temperatures through dynamic voltage tuning would further enhance the energy savings provided with the proposed techniques.

5. CONCLUSIONS

Gate overdrive variation with temperature dominates the speed characteristics of deeply scaled CMOS circuits. The propagation delay is reduced with the increased temperature in a 32nm CMOS technology, indicating a complete reversal in the temperature dependent speed characteristics of nanometer CMOS circuits. The reversal in the temperature dependent speed characteristics provides new opportunities to lower the active mode energy consumption at high temperatures. Temperature-adaptive dynamic supply and threshold voltage tuning techniques are proposed in this paper to reduce the high temperature energy consumption without degrading the circuit speed in active CMOS circuits.

The temperature-adaptive voltage scaling technique dynamically adjusts the power supply voltage of a circuit based on the die-temperature fluctuations. The high temperature energy consumed with the temperature-adaptive voltage scaling technique is 19.1% to 21% lower as compared to the energy consumed at the standard nominal supply voltage. Alternatively, the temperature-adaptive body-bias technique dynamically tunes the threshold voltages of the devices based on the fluctuations of the die temperature and the circuit speed. The high temperature active mode energy is reduced by up to 29.8% with the temperature-adaptive reverse body-bias technique as compared to the standard zero body-biased circuits. Dynamically increasing the threshold voltages of the devices through temperature-adaptive reverse body-bias is shown to be very effective to reduce the high temperature energy consumption while maintaining constant speed in the active mode in deeply scaled nanometer CMOS integrated circuits experiencing significant die-temperature fluctuations.

REFERENCES