Low-Power Low-Voltage Hot-Spot Tolerant Clocking with Suppressed Skew

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Abstract — A methodology based on supply voltage optimization for lowering the power consumption and temperature fluctuations induced skew of clock distribution networks is proposed in this paper. The clock signal is distributed globally at a lower optimum supply voltage. To maintain the speed of the system, a dual supply voltage (dual-V_{th}) clock distribution network is presented. Level converters are utilized to restore the standard full swing clock signal at the leaves of the low voltage clock distribution network. A novel level converter with low skew, propagation delay, and power consumption characteristics is presented. The optimum supply voltage that minimizes clock skew is 44% lower than the nominal supply voltage in a 0.18µm CMOS technology. The temperature fluctuations induced skew and power consumption of the proposed dual-V_{th} clock distribution network are 74% and 50.8% lower, respectively, as compared to a standard clock distribution network operating at the nominal supply voltage.

I. INTRODUCTION

Clock distribution network consumes a significant portion of the power, area, and metal resources of an integrated circuit (IC). Technology scaling coupled with the increase in die size and clock frequency causes the process and environment parameter variations to be more pronounced [1]. Coping with parameter variations is particularly challenging in the design of the clock distribution networks since the clock signal needs to be distributed to the entire IC with controlled skew. Clock skew degrades the performance of an IC by reducing the time available for computation in each clock cycle.

The increasing operating frequency and growing die size increase the power consumption of the clock distribution network while shrinking the budget for clock skew with each new technology generation. The imbalanced utilization and diversity of circuitry and the increasing power consumption cause temperature gradients across an IC, thereby leading to an increase in the clock skew. The two primary issues in the design of the clock distribution networks are the higher power consumption and the increased clock skew due to parameter variations in today’s high performance integrated circuits.

In [2], programmable delay elements are employed for reducing the skew induced by process parameter variations in a clock distribution network. This approach is ineffective for reducing the clock skew caused by environment variations since a significant amount of time is required for reprogramming. In [3] and [4], delay elements are programmed dynamically using phase detectors in a clock distribution network. This approach, although potentially effective in reducing the deviations in circuit characteristics induced by both process and environment parameter variations, suffers from higher design complexity, area, power consumption, and clock jitter.

Low-swing clocking is proposed in [5] and [6] to reduce the power consumption at the expense of increased clock skew. In [5], the effect of temperature fluctuations on clock skew is not considered. In [6], the clock distribution network becomes more sensitive to temperature variations. The weaker driving capability of the low voltage buffers requires increasing either the number or the size of the buffers to maintain the clock signal skew rate in a low swing clock distribution network. The overhead associated with buffer redesign is not discussed in [5] and [6].

The effect of on-chip temperature gradients on clock skew is characterized in this paper. Supply voltage optimization is demonstrated to be an effective method to reduce the power consumption and minimize the clock skew induced by temperature fluctuations in a clock distribution network. The clock signal is distributed at a lower optimum supply voltage with the proposed scheme. To maintain the performance of the system, the clock signal is restored to the standard voltage level by employing level converters at the leaves of the clock distribution network. A novel level converter with low skew, propagation delay, and power consumption characteristics is also proposed in this paper.

The paper is organized as follows. The impact of temperature variations on the delay of CMOS gates and wires is characterized in Section II. The proposed supply voltage optimization technique is applied to a clock distribution network in Section III. The simulation results characterizing the skew and power consumption of a dual-V_{th} clock distribution network with a new level converter based on a dual threshold voltage CMOS technology are presented in Section IV. Finally, conclusions are provided in Section V.

II. TEMPERATURE IMPACT ON DELAY

In this section the impact of temperature on the propagation delay of CMOS circuits (including wires) is presented. The impact of temperature on the circuit delay is studied in [9]. The delay of a CMOS gate is affected by two primary temperature-dependent parameters, the carrier mobility μ and the threshold voltage V_{th}. Both μ and V_{th} decrease as the temperature increases [9]. The degradation of mobility tends to increase the delay. Alternatively, the decrease in the absolute value of the threshold voltage tends to lower the delay. The combined effect of the mobility and threshold voltage variations on the propagation delay depends on other parameters such as the supply voltage and the input signal slope.

Variations in gate overdrive are smaller as compared to carrier mobility variations when the temperature fluctuates in circuits operating at the nominal supply voltage in a 0.18µm CMOS technology as described in [9]. The transistor saturation current and the circuit speed, therefore, degrade with the increased temperature. A design methodology based on scaling the supply voltage for suppressing the MOSFET current variations due to temperature fluctuations is proposed in [9]. In order to compensate for the variations of carrier mobility, the sensitivity of gate overdrive to temperature fluctuations is enhanced by lowering the supply voltage.

At the optimum supply voltage, the gate overdrive variation completely counterbalances the variation of carrier mobility, thereby producing a constant MOSFET current insensitive to temperature fluctuations.

In addition to the active devices, accurate modeling of the temperature dependence of the parasitic impedances of wires is also critical in deep submicrometer CMOS technologies. The widths of the wires are scaled in order to enhance the integration density in each new technology generation. The increasing resistance of the wires plays an important role in determining the performance of CMOS integrated circuits. The effect of temperature on wire delay is...
not taken into consideration in [9]. In clock distribution networks, long wires with significant resistance are employed, making the effect of temperature on wire resistance and delay more pronounced. Resistance of a metal wire increases approximately linearly with the temperature. The signal propagation delay along a wire, therefore, increases at higher temperature. The temperature dependence of the wire impedances as well as the device parameters are considered in this paper for an accurate characterization of the effect of temperature fluctuations on clock skew.

A significant number of repeaters is employed in order to maintain the signal integrity and to reduce the short-circuit power by controlling the transition time of the clock signal in a clock distribution network. The delay of the clock signal from the root to the leaves of the clock distribution network is composed of a series of gate and wire delays. Due to the formation of on-chip hot spots, paths emerging from the root of a clock distribution network pass through different temperature zones as illustrated in Fig. 1. Significant clock skew is induced by these temperature gradients in a standard clock distribution network operating at the nominal supply voltage. For maintaining the system performance and reliability, eliminating the sensitivity of the clock distribution network to the temperature fluctuations is highly desirable.

III. SUPPLY VOLTAGE OPTIMIZATION IN CLOCK DISTRIBUTION NETWORKS

The proposed supply voltage optimization methodology is presented in this section. The strength of the technique lies on counterbalancing the mobility variations with the gate overdrive variations at the device level by operating a clock distribution network at an optimum lower supply voltage. The supply voltage optimization technique thereby effectively suppresses the temperature fluctuations induced clock skew regardless of the on-chip temperature profile and the employed buffer insertion and sizing algorithm.

A two level buffered H-tree clock distribution network spanning a 20mm × 20mm die is used in the evaluation of the proposed methodology as shown in Fig. 1. The target clock frequency is 1 GHz. The thick and thin lines in Fig. 1 represent the first (routed in the topmost metal layer) and the second (routed in the second topmost metal layer) levels, respectively, of the clock distribution network. Each branch in the first (second) level is 5mm (2.5mm) long. Each wire segment between two buffers is modeled as a 22 RC network. The wire width is 1µm (0.5µm) in the first (second) topmost metal layer. The wire thickness is 1µm. The spacing between wires is 1µm. The sheet resistance is 0.0232 Ω/µm. Buffer insertion and sizing are carried out using an iterative Spice-based algorithm. The objective of the algorithm is to minimize the power consumption while constraining the transition times of the clock signal at the leaves of the clock tree to be less than 10% of the clock period.

The H-tree clock distribution network is designed at the nominal supply voltage assuming a uniform worst case die temperature (125 °C). The supply voltage is then scaled by steps of 0.1V. The sizes of the buffers in the clock tree are increased to meet the transition time constraints at each supply voltage assuming a uniform die temperature of 125 °C. Each clock distribution network operating at a specific supply voltage is then characterized for skew that would be caused by a non-uniform die temperature profile. The temperature profile assumed in this paper is illustrated in Fig. 1. For each network operating at a different supply voltage, the maximum clock skew between the leaves of the clock distribution network and the average power consumption are evaluated.

The maximum clock skew between the leaves of the clock distribution network versus the supply voltage is plotted in Fig. 2. The temperature gradient induced skew is 35ps with the standard clock distribution network operating at the nominal supply voltage (V_{DD}-nominal = 1.8V). When the supply voltage is scaled to 1.7V, the clock skew slightly increases (by 1ps) due to the enhanced mobility variations at lower supply voltages [9]. Further supply voltage scaling reduces the clock skew as the enhanced gate overdrive variations effectively counterbalance the mobility fluctuations. There is an optimum supply voltage (V_{DD}-optimum = 1V) at which the temperature fluctuations induced clock skew is minimized as shown in Fig. 2. The clock skew at the optimum supply voltage is 7ps. Temperature fluctuations induced clock skew is reduced by 80% with the proposed supply voltage optimization scheme.

The variation of the normalized power consumption with the supply voltage is shown in Fig. 3. Buffer sizes are increased at the lower supply voltages to maintain the signal rise and fall times within 10% of the clock period. Hence the reduction in average power consumption with the scaling of the supply voltage is less than quadratic. As the supply voltage is scaled, the power overhead of the larger buffers eventually exceeds the power savings obtained by reducing the supply voltage. There is therefore an optimum supply voltage that minimizes the power consumption. The optimum supply voltage (V_{DD}-optimum = 1V) that minimizes the temperature fluctuations induced skew also minimizes the power consumption for this specific clock distribution network, as shown in Figs. 2 and 3. A 53.8% reduction in the average power consumption is observed at the optimum supply voltage with the proposed technique.
IV. LEVEL CONVERTERS

Level converters are employed at the leaves of the dual-VDD clock distribution network in order to restore the standard full-swing clock signal for maintaining the system performance. The issues in the design of voltage level converters are discussed in this section. A new dual threshold voltage level converter that is robust against temperature fluctuations is introduced.

A standard level converter circuit is shown in Fig. 4. Provided that the upper boundary of the input voltage swing is reduced, the standard voltage interface circuit insures that the low swing input signal does not drive a PMOS transistor directly. Due to the transitory contention between the pull-up and the pull-down networks and the increased size of the NMOS transistors to compensate for the degraded gate overdrive, however, the standard level converter consumes significant power.

Another level converter (LC2) is proposed in [7] to enhance the level conversion speed. LC2 is shown in Fig. 5. When the input (A) switches from 0V to VDDL, there is a direct current path from VDDH to GND through the M2-M3 path. This direct current path is active until Node1 is charged to VDDH through M4 and M5. Similarly, when the input switches from VDDL to 0V, there is a direct current path from VDDH to GND through the M5-M4-M1 path. This direct current path is active until Node2 is pulled up to VDDH and M4 is turned off. LC2 therefore consumes significant short-circuit power. Furthermore, the propagation delay of LC2 is highly sensitive to temperature fluctuations. Employing LC2 with the proposed dual-VDD clock distribution network produces significant clock skew between the final stages of the network despite the optimization of the supply voltage.

In this paper a new low power level converter that is robust against temperature fluctuations is proposed. Dual threshold voltage devices are employed in order to simultaneously suppress the static DC current and the temperature fluctuations induced skew of the new level converter. The proposed level-converter is shown in Fig. 6. The purpose of M1 is to isolate the two power supplies when the input is at VDDL. For this purpose the voltage of Node2 is restricted to be below VDDL + Vthn. M4 guarantees that the voltage of Node2 does not exceed VDDL + Vthn. M1 maintains the voltage of Node2 at VDDH - Vthn assuming Vthn < VDDH - VDDL < 2Vthn. The capacitor (C = 6fF) stabilizes the voltage of Node2 against coupling disturbances from the input and the surrounding active areas. M1, M4, and the capacitor enhance the speed of the circuit.

The level converter (LC3) operates as follows. When the input (A) is at 0V, Node1 is pulled high to VDDL turning M2 off (note that M2 is a high-\(|V_{th}\)| device). The output node is discharged to 0V through the pass transistor M1. When the input transitions to VDDL, the output node is initially charged to approximately VDDH - 2Vthn through M1. M2 is turned on after the high-to-low propagation delay of the inverter (I1). The output is pulled all the way up to VDDH through M2. M1 is eventually turned off isolating the two power supplies. Both M1 and M2 assist the output low-to-high transition, thereby eliminating the contention current and enhancing the speed. The small transistor count and the elimination of the feedback mechanism reduce the power consumption of the proposed level converter as compared to the previously published circuits.
producing a temperature variation insensitive constant drain current.

1 is connected to the optimum supply voltage (VDDL) for insensitivity to temperature variations. The gate voltage of M1 is higher than VDDL. Due to the body effect, however, the gate overdrive voltage of M1 is close to the optimum value required for producing constant current under temperature variations. M1 is connected to VDDH. Similar to the optimization of the supply voltage, the sensitivity of the drain current to temperature fluctuations can also be suppressed by optimizing the threshold voltage of a MOSFET [8]. The threshold voltage of M2 is individually optimized for temperature variation insensitive constant drain current (High-Vth = -0.96V). The proposed level converter thereby displays weaker propagation delay sensitivity to temperature fluctuations. The reduced power consumption and the relative insensitivity to temperature variations make LC3 preferable for the proposed dual-VDD clock distribution network.

Each level converter is sized to achieve minimum average power consumption using the HSPICE built-in optimizer. The proposed low swing clock distribution network is integrated with the level converters at the leaves of the clock tree for restoring the standard full voltage swing (0 → VDDH) clock signal. Simulations are carried out with the proposed low swing clock distribution network operating at the optimum supply voltage (CDN-optimum) and the standard clock distribution network operating at the nominal supply voltage (CDN-standard). The normalized average power consumption and the overall temperature fluctuations induced clock skew of the entire clock tree including the voltage level converters and power consumption are reduced by 74% and 50.8%, respectively, with the proposed technique as compared to the standard clock distribution network operating at the nominal supply voltage.

Table I Normalized Average Power Consumption and Temperature Fluctuations Induced Skew with the Level Converters.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Normalized Average Power (%)</th>
<th>Clock Skew (ps)</th>
<th>Rising Edge</th>
<th>Falling Edge</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDN-standard</td>
<td>100</td>
<td>35</td>
<td>32.5</td>
<td></td>
</tr>
<tr>
<td>CDN-optimum with LC1</td>
<td>52</td>
<td>15</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>CDN-optimum with LC2</td>
<td>50.6</td>
<td>21</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td>CDN-optimum with LC3</td>
<td>49.2</td>
<td>9</td>
<td>9</td>
<td></td>
</tr>
</tbody>
</table>

The supply voltage fluctuation is another significant source of uncertainty in today’s ICs. The impact of supply voltage variations on the power consumption and the temperature fluctuations induced skew are also evaluated in this paper, as listed in Table II. In the first two entries of the table, the supply voltages of the standard and the proposed optimum clock distribution networks (without level converters) are varied by ±10%. The power and temperature fluctuations induced clock skew of each network are measured. In the last entry of the table, the dual supply voltages of the proposed clock distribution network (integrated with the proposed level converter, LC3) are varied. The worst case combination of VDDH and VDDL that maximizes the power consumption and the temperature fluctuations induced skew is reported.

As listed in Table II, the proposed design methodology maintains its effectiveness in the presence of supply voltage variations. The worst-case power consumption and temperature variation induced skew of the optimum clock distribution network with the level converters is 50.7% and 44% lower as compared to the worst-case power consumption and skew of the standard design, respectively.

V. CONCLUSIONS

A design methodology based on supply voltage optimization is proposed in this paper for reducing the power consumption and minimizing the temperature fluctuations induced skew of clock distribution networks. The clock signal is distributed globally at a lower optimum supply voltage. The optimum supply voltage that minimizes clock skew is 44% lower than the nominal supply voltage in a 0.18µm CMOS technology. To maintain the system performance, the standard full swing clock signal is restored using voltage interface circuits near the leaves of the dual-VDD clock distribution network.

A new low-power dual threshold voltage level converter that is robust against temperature fluctuations is presented. With the proposed dual-VDD clock distribution network, the temperature fluctuations induced clock skew and power consumption are reduced by 74% and 50.8%, respectively, as compared to a standard clock distribution network operating at the nominal supply voltage. The effectiveness of the proposed methodology for reducing skew and power consumption is also verified in the presence of significant supply voltage variations.

Table II Effect of Supply Voltage Variation on Power Consumption and Temperature Fluctuations Induced Skew.

<table>
<thead>
<tr>
<th>Supply Voltage (V)</th>
<th>Average Power (mW)</th>
<th>Clock Skew (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Rising Edge</td>
<td>Falling Edge</td>
</tr>
<tr>
<td>1</td>
<td>1.98</td>
<td>16.5</td>
</tr>
<tr>
<td>1.8</td>
<td>13.44</td>
<td>35</td>
</tr>
<tr>
<td>1.62</td>
<td>10.7</td>
<td>36</td>
</tr>
<tr>
<td>1.1</td>
<td>6.6</td>
<td>19</td>
</tr>
<tr>
<td>1</td>
<td>6.2</td>
<td>7</td>
</tr>
<tr>
<td>0.9</td>
<td>6.4</td>
<td>16</td>
</tr>
<tr>
<td>3 VDDL = 1.98 VDDL = 1.1</td>
<td>8.13</td>
<td>20</td>
</tr>
</tbody>
</table>

REFERENCES