Supply and Threshold Voltage Optimization for Temperature Variation Insensitive Circuit Performance: A Comparison

Ranjith Kumar and Volkan Kursun
Department of Electrical and Computer Engineering
University of Wisconsin – Madison, Madison, Wisconsin 53706-1691

Imbalanced utilization of circuitry at different sections of an integrated circuit and fluctuations in the environmental temperature can cause significant variations in the die temperature [1]. Fluctuations in the die temperature affect the device characteristics thereby varying the performance of an integrated circuit. In this paper, the supply and threshold voltage optimization techniques to achieve temperature variation insensitive circuit performance are compared. The speed and energy tradeoffs with the two optimization techniques are presented.

An increase in the die temperature degrades the absolute values of threshold voltage and carrier mobility. Threshold voltage degradation with temperature tends to enhance the drain current because of the increase in gate overdrive $|V_{GS} - V_{T}(T)|$. Alternatively, degradation in carrier mobility tends to lower the MOSFET drain current. Effective variation of the MOSFET drain current is determined by the variation of the dominant device parameter when the temperature fluctuates [2]-[3].

Gate overdrive and carrier mobility variations due to temperature fluctuations for devices with the nominal supply and threshold voltages in a 65nm CMOS technology (VDD = 1.0V and $|V_{T}(T_0)| = 0.22V$) are presented in Table I. The variation of the drain current ($I_{DS}$) with supply voltage ($V_{DD}$) and temperature for MOSFETs in a 65nm CMOS technology is shown in Fig. 1. As listed in Table I, variations of gate overdrive are smaller as compared to carrier mobility variations when the temperature fluctuates. The MOSFET drain current, therefore, degrades when the temperature is increased from 25°C to 125°C, as shown in Fig. 1. Propagation delay variations with temperature for circuits operating at the nominal supply and threshold voltages are shown in Fig. 2. Circuit speed at nominal voltages degrade by up to 54.5% when the temperature is increased from 25°C to 125°C, as shown in Fig. 2.

The above results indicate that operating an integrated circuit at the prescribed nominal supply and threshold voltages is not preferable for reliable circuit operation under temperature fluctuations. In order to compensate for the variation of carrier mobility, the sensitivity of gate overdrive to temperature fluctuations should be enhanced. Scaling the supply voltage increases the sensitivity of the gate overdrive to temperature fluctuations [3]. At the optimum supply voltage, the temperature fluctuation induced gate overdrive variation completely counterbalances the variation of carrier mobility. A transistor biased at this optimum supply voltage, therefore, produces a temperature variation insensitive constant drain current, as shown in Fig. 1.

An alternative technique is to optimize the threshold voltages for temperature variation insensitive performance at a fixed supply voltage. For circuits operating at the nominal supply voltage, the sensitivity of the gate overdrive to temperature fluctuations can be enhanced by increasing the device threshold voltage. The variation of the drain current ($I_{DS}$) with threshold voltage ($V_{T}$) and temperature for devices operating at the nominal supply voltage in a 65nm CMOS technology is shown in Fig. 3. At the optimum threshold voltage, temperature fluctuation induced gate overdrive variation counterbalances the variation of carrier mobility. Similar to the optimum supply voltage operation, MOSFETs operating at the optimum threshold voltage produce temperature variation insensitive constant drain current, as shown in Fig. 3.

The propagation delay at the optimum supply and threshold voltages for circuits in a 65nm CMOS technology are shown in Figs. 4 and 5, respectively. The optimum supply voltages that yield a temperature variation insensitive performance are 67% to 69% lower than the nominal supply voltage. Alternatively, the optimum threshold voltages are 4.2x to 4.3x higher than the nominal device threshold voltage. At the optimum supply and threshold voltages, the circuit speed is degraded by up to 17.9x and 428x, respectively, as compared to the speed at the nominal voltages.

Higher supply voltages are preferable in speed critical applications. For circuits operating at the nominal supply voltage, however, the potential speed gains in using a higher supply voltage are diminished by the threshold voltage optimization technique. Furthermore, energy savings achieved with the threshold voltage optimization technique is also lower as compared to the supply voltage optimization technique. Optimizing the supply voltages is therefore preferable as compared to the threshold voltage optimization technique in order to eliminate the delay sensitivity to temperature fluctuations.

**CONCLUSIONS**

Two design methodologies for temperature variation insensitive speed are compared in this paper. Circuits display a temperature variation insensitive performance when operated at a supply voltage 67% to 69% lower than the nominal supply voltage. Similarly, the circuits operating at the nominal supply voltage are insensitive to temperature variations when the device threshold voltage is 4.2x to 4.3x higher than the nominal threshold voltage. The energy reduction provided by the supply voltage optimization technique is higher as compared to the threshold voltage optimization technique. The supply voltage optimization technique is shown to be more effective in achieving temperature variation tolerant low power CMOS circuits with a smaller speed penalty.
REFERENCES

TABLE I
GATE OVERDRIVE AND CARRIER MOBILITY VARIATIONS AT THE NOMINAL SUPPLY AND THRESHOLD VOLTAGES

<table>
<thead>
<tr>
<th>Technology</th>
<th>Gate Overdrive (V)</th>
<th>Carrier Mobility (x10^3 m^2/Vs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMOS</td>
<td>NMOS</td>
<td>PMOS</td>
</tr>
<tr>
<td>65nm CMOS Technology</td>
<td>-0.78</td>
<td>0.78</td>
</tr>
<tr>
<td>25°C</td>
<td>-0.82</td>
<td>0.82</td>
</tr>
<tr>
<td>Variation (%)</td>
<td>4.71</td>
<td>4.71</td>
</tr>
</tbody>
</table>

![Fig. 1](image1.png)

Fig. 1. Variation of MOSFET drain current ($I_{DS}$) with supply voltage ($V_{DS}$) and temperature. $|V_{DS}| = |V_{GS}| = V_{DD}$ and $|V_{t(T0)}| = 0.22V$.

![Fig. 2](image2.png)

Fig. 2. Temperature fluctuation induced propagation delay variations for circuits operating at the nominal supply and threshold voltages. $V_{DD} = 1.0V$ and $|V_{t(T0)}| = 0.22V$.

![Fig. 3](image3.png)

Fig. 3. Variation of MOSFET drain current ($I_{DS}$) with threshold voltage ($V_t$) and temperature. $|V_{DS}| = |V_{GS}| = V_{DD} = 1.0V$.

![Fig. 4](image4.png)

Fig. 4. Optimum supply voltages providing temperature variation insensitive propagation delay. $|V_{t(T0)}| = 0.22V$.

![Fig. 5](image5.png)

Fig. 5. Optimum threshold voltages providing temperature variation insensitive propagation delay. $V_{DD} = 1.0V$.

![Fig. 6](image6.png)

Fig. 6. Normalized energy per switching cycle at different voltages.